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**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS:**

Claims 1-4 (canceled).

Claim 5 (original): A process for fabricating an integrated circuit package, comprising:

establishing a plating mask on a first surface of a metal carrier, the plating mask defining a plurality of components including at least one die attach pad, at least one row of contact pads and at least one additional electronic component;

depositing a plurality of metallic layers on exposed portions of said first surface of said metal carrier, thereby forming said plurality of components;

stripping said plating mask from said metal carrier and leaving said plurality of metallic layers in the form of said plurality of components;

mounting at least one semiconductor die to a respective one of said at least one die attach pad such that each die attach pad has a respective semiconductor die mounted thereon and pads of each said respective semiconductor die are electrically connected to ones of said contact pads and to said at least one additional electronic component;

overmolding said first surface of said metal carrier to encapsulate said plurality of components and said at least one semiconductor die; and

etching away said metal carrier.

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Claim 6 (original): The process according to claim 5, wherein etching away said metal carrier includes etching a first one of said metallic layers, thereby providing indentations at each of said plurality of components.

Claim 7 (original): The process according to claim 6, further comprising solder mask printing to cover passive ones of said components and leaving exposed portions of said components in ones of said indentations.

Claim 8 (original): The process according to claim 7, wherein said solder mask printing forms a pattern for solder ball attachment to said at least one die attach pad and said contact pads and said process further comprises fixing a plurality of solder balls at said exposed portions of said components.

Claim 9 (original): The process according to claim 5, wherein said at least one additional electronic component is selected from the group consisting of at least one capacitor, at least one inductor and both a capacitor and an inductor.

Claim 10 (original): The process according to claim 5, wherein said establishing a plating mask comprises establishing a plating mask on a first surface of a metal carrier, the plating mask defining a plurality of components including two die attach pads, at least one row of contact pads, an inductor and a capacitor.

Claim 11 (original): The process according to claim 10, wherein said inductor and said capacitor are disposed between said die attach pads.

Claim 12 (original): The process according to claim 5, wherein said mounting at least one semiconductor die comprises:

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mounting each said at least one semiconductor die to said respective one of said at least one die attach pad; and

wire bonding each said at least one semiconductor die to ones of said contact pads and to said additional electronic component.

Claim 13 (original): The process according to claim 5, wherein in said establishing a plating mask on said first surface of a metal carrier, said plurality of components further includes a circuit pattern of traces extending from said at least one row of contact pads to ends proximal said die attach pad.

Claim 14 (original): The process according to claim 13, wherein in said establishing a plating mask on said first surface of a metal carrier, said additional electronic component comprises at least one capacitor and said circuit pattern further includes a respective trace extending in from each said at least one capacitor, to an end proximal said die attach pad.

Claim 15 (original): The process according to claim 14, wherein said mounting at least one semiconductor die comprises:

mounting each said at least one semiconductor die to said respective one of said at least one die attach pad; and

wire bonding each said semiconductor die to ones of the traces.

Claim 16 (original): The process according to claim 14, wherein said mounting at least one semiconductor die comprises:

mounting each said at least one semiconductor die in a flip chip orientation to said respective one of said at least one die attach pad such that pads of said semiconductor die are electrically connected to ones of said traces.

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Claim 17 (original): The process according to claim 5, further comprising singulating to isolate said integrated circuit package from other packages.

Claim 18 (original): The process according to claim 5, wherein depositing a plurality of metallic layers on exposed portions of said first surface of said metal carrier, includes further masking between depositing of said metallic layers to thereby selectively plate.

Claim 19 (original): The process according to claim 5, wherein said establishing a plating mask comprises:

depositing a photo-imageable mask on the first surface of the metal carrier;

imaging said mask to provide imaged portions that define the desired electronic component; and

developing said mask to remove the imaged portions of the mask.

20-30 (canceled).